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Design and Analysis of Data Path Elements using Low Power State Retention Technique

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Abstract: Most of the portable systems, such as cellular communication devices, and laptop computers operate from a limited power supply. The extension of battery-based operation time is a significant design goal which can be made possible by controlling the leakage current flowing through the CMOS circuit. Leakage power loss is critical in CMOS VLSI circuits as it leaks the battery even when the devices are in idle state. In this work a new circuit technique called LPSR technique is proposed to reduce threshold leakage power as well as total power in CMOS circuits. This proposed technique reduces maximum amount of leakage power during deep sleep mode, maximum power during dynamic mode and a provision of preserving state in low power sleep mode. Finally earlier well known techniques for leakage reduction and state retention are compared with this technique. Circuit designing, simulation and low power performance evaluation is done using CMOS technology files in Tanner EDA tool.

Keywords: Dynamic Power, Leakage Current, Low Power State Retention (LPSR), Power Dissipation, State Retention, Static Power.

I. INTRODUCTION

In the increasing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as mobile phones, notebook computers, hearing aids etc. has to be realized with very low power requirements. The power dissipation has become a very critical design issue due to device miniaturization and rapid growth towards wireless communication. The larger the battery lasts; the better is the device. The power dissipation has not diminished even with the scaling down of the supply voltage. The technology scaling resulted in the use of lower power supply voltage for CMOS circuits which has an associated effect of lower threshold voltages to enhance performance. As the transistors cannot be switched-off completely, lower threshold voltage results in exponential rise in leakage current [1]. Since the channel length for the successive technology generations is reducing, threshold voltage and gate-oxide thickness are also being scaled down to keep pace with the performance. The total power dissipation includes dynamic and static components.

The dynamic power consumption is mainly due to the charging and discharging of the capacitance and short circuit current. Dynamic power is directly proportional to the square of the supply voltage. Therefore, dynamic power reduced in a quadratic manner when the supply voltage (VDD) is reduced.

Leakage power is dependent on the leakage current flowing in the CMOS. The components of static power dissipation are sub-threshold leakage, gate oxide leakage, junction leakage, gate induced drain leakage, and punch through leakage. In CMOS inverter ideally current flows from source-to-drain, when VGS > VT. In real transistors current does not abruptly cut-off below threshold, but drops off exponentially as given by equation (1). This sub-threshold leakage current for VGS < VT is given by,

$$I_{DS} = I_{DS_0} e^{(V_{GS} - V_T)/(nV_T)} [1 - e^{(V_{DS}/V_T)}] \quad (1)$$

Where,

$$V_T = V_{T_0} - \eta V_{DS} + \gamma \left[(\phi_S + V_{SB})^{0.5} - (\phi_S)^{0.5} \right] \quad (2)$$

In above equations, I_{DS0} is current at threshold, γ is the body effect coefficient, η represents the effect of drain-to-source voltage (V_{DS}) on threshold voltage, n is the sub-threshold swing coefficient, VT_0 is the zero bias threshold voltage, VT is the thermal voltage respectively. The η term describes Drain Induced Barrier Lowering (DIBL). Sub-threshold conduction is enhanced by DIBL in which positive V_0 effectively reduces VT. Leakage current doubles for every 8˚ to 10˚ rise in temperature. The sub-threshold leakage current can be reduced by increasing threshold voltage VT_0, increasing V_{SB} and reducing V_{GS}, V_{DS} and lowering the temperature.

Many leakage power control techniques uses the methods such as scaling supply voltage, reducing voltage swing and capacitance, reduction of switching activity or introducing high resistance between the supply voltage and ground. LECTOR [4], GALEOR [5], Sleepy Keeper [6], Sleepy Pass Gate [8] are some of the techniques for leakage reduction. Each method has its own merits and demerits. Some techniques use dual VT transistor; a high VT transistor to reduce leakage and a low VT transistor to improve the speed of operation in critical sections of the circuit.

The design and analysis of the LPSR technique is proposed in this paper to reduce leakage power and total power in data path elements, which makes use of single

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VT transistors in all parts of the circuit with the target to achieve low leakage power during sleep mode of operation and lower dynamic power dissipation.

II. LITERATURE REVIEW

The review of earlier work done for leakage reduction and state retention are stated in this section.

A. N. Hanchate and N. Ranganathan
"Lector: A technique for leakage reduction in CMOS circuits". Fig.1 shows the block diagram of Lector technique. In this technique author introduce two leakage control transistors (a p-type and n-type) within the logic circuit for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. In this arrangement, one of the LCTs is always "near its cut-off voltage" for any input combination. This increases the resistance of the path from VDD to ground, leading to significant decrease in leakage currents.

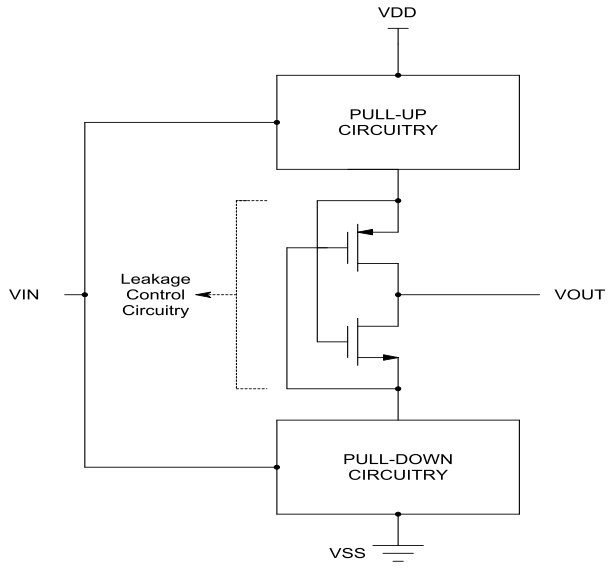

Fig. 1. LECTOR Technique

B. Shrikanth Katrue and Dhireesha Kudithipudi
"GALEOR: Leakage reduction for CMOS circuits". Fig.2 shows the block diagram of GALEOR technique. In GALEOR technique the author introduced stacking effect in the circuit results reduction in leakage current flowing across circuit. In this approach, one gate leakage high VT NMOS transistor is introduced between the output and the pull-up network and another gated leakage high VT PMOS transistor is inserted between output and pull-down network. Due to the threshold voltage loss caused by high VT MOS transistors, this technique suffers from significant low voltage swing where low logic level appears much above than 0 and high level occurs much below than VDD. It results higher propagation delay due to low output voltage swing.

These two LECTOR and GALEOR techniques have very good low leak operation but there is no provision of sleep mode of operation.

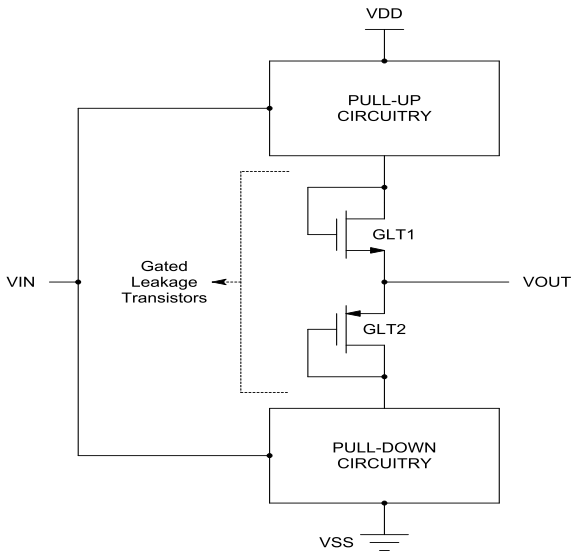

Fig. 2. GALEOR Technique

C. M. Geetha Priya, K. Baskaran and D. Krishnaveni
"A novel leakage power reduction technique for CMOS VLSI circuits". Fig.3 shows the block diagram of Sleepy Pass Gate technique. In this Sleepy Pass Gate approach author inserted two sleep transistors PMOS and NMOS connected in parallel between pull-up and pull-down networks of a CMOS circuit to form a pass gate like structure. This technique has large power dissipation during pulsed operation.

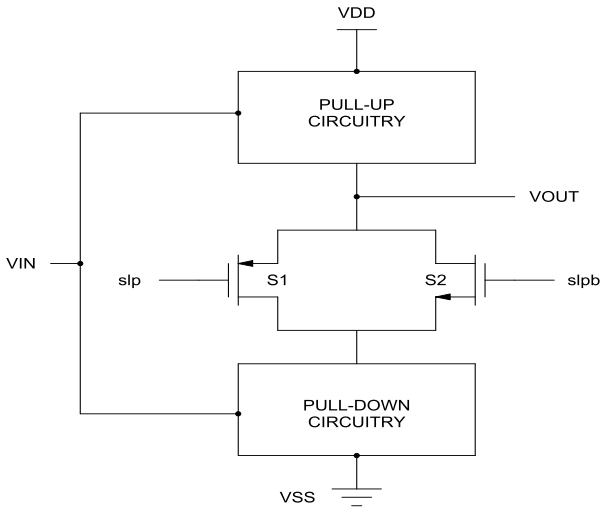

Fig. 3. Sleepy Pass Gate Technique

D. S. H. Kim and V. J. Mooney
"Sleepy keeper: a new approach to low leakage power VLSI design". Fig.4 shows the block diagram of Sleepy Keeper technique. In this work, author inserted parallel connected combination of PMOS and NMOS transistors between pull-up circuitry and supply voltage (VDD), and pull-down circuitry and ground (VSS). In sleep mode, this additional NMOS transistor is the only source of VDD to the pull-up circuitry and additional PMOS transistor is the only source of ground to the pull-down circuitry since the sleep transistor is off. This technique uses extra retention

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transistors to maintain logic state during sleep mode but results in large power dissipation during clocked operation.

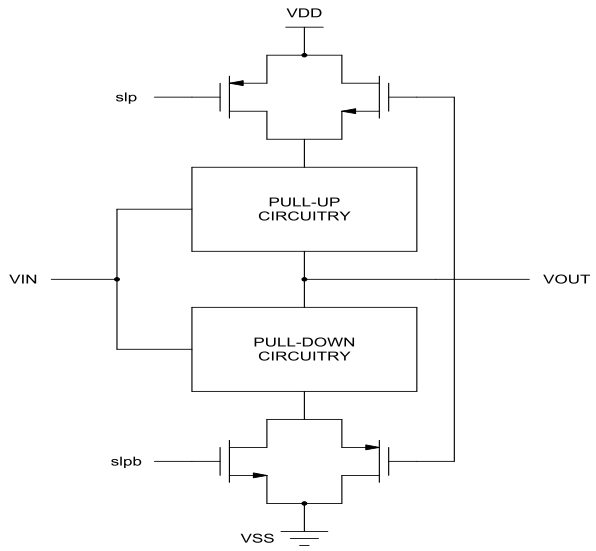

Fig. 4. Sleepy Keeper Approach

III. PREVIOUS WORK

As per the literature review, even though the above discussed techniques reduce the power dissipation, this techniques are unable to retain state during sleep operation. So, to retain the logical output state even in the sleep mode and to reduce the power consumption to a maximum possible extent a new Low Power State Retention (LPSR) technique is proposed in this paper.

IV. PROPOSED METHODOLOGY

LPSR Technique:-

The LPSR technique is proposed in this section to reduce the leakage power and total power dissipation to a maximum possible extent.

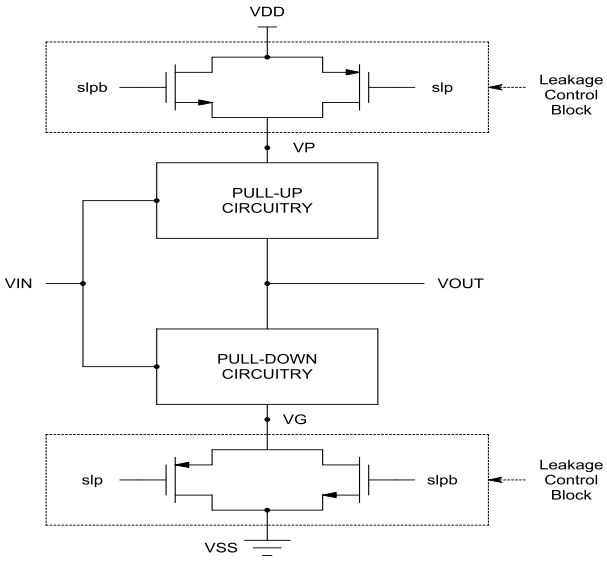

Fig. 5. Generic LPSR Circuit

The LPSR technique makes use of a pair of NMOS and PMOS transistors in the pull-up and pull-down paths of a CMOS circuit. Fig.5 shows the general block diagram of LPSR circuit.

The sleep transistor is referred to be either a PMOS or NMOS high VT transistor that connects a permanent power supply (VDD) to the circuit power supply which is commonly called as "virtual power supply". The PMOS transistor is used to switch on VDD and NMOS transistor is used to control VSS supply. The sleep control transistors are controlled by a power management unit to switch ON and OFF power supply.

As per the literature review, even though the above discussed techniques reduce the power dissipation, this techniques are unable to retain state during sleep operation.

So, to retain the logical output state even in the sleep mode and to reduce the power consumption to a maximum possible extent a new Low Power State Retention (LPSR) technique is proposed in this paper.
This technique has four modes of operation:

A. Active Mode

Two sleep control signals namely slp = 0 and slpb = 1 are used to switch on the sleep transistors in leakage control block. Thus the virtual ground node VG is at ground potential and the virtual power node VP is at VDD. The circuit thus sees good potential difference across nodes VP and VG. The circuit functions as per the truth table with good output logic levels.

B. Deep Sleep Mode

Both the sleep control signals are held at slp = 1 and slpb = 0 states to switch off all the sleep transistors in both pull up and pull down leakage control blocks. Thus the actual power and ground path are disconnected virtually and the circuit experiences lower voltage across the nodes VP and VG.

A very high resistance path is established between the VDD and VSS due to parallel combination of OFF resistance of sleep transistors and the leakage current flowing through circuit reduces significantly and hence will dissipate lowest power.

C. State Retention Mode 1

The sleep signals are maintain at slp = 0 and slpb = 0. The circuit sees a voltage higher than ground at the node VG and full VDD at the node VP. The state retention takes place with low leakage current with the output at good logic '1' level.

D. State Retention Mode 0

The sleep control signals are maintain at slp = 1 and slpb=1. The connection to actual ground is complete, the node VP is at lower VDD. Thus the state retention takes place with low leakage current with the output at good logic '0' level.

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Data Path Elements:-

The LPSR technique is applied to 2X1 Multiplexer and Full Adder. The performance is compared with all other techniques. The schematic of the circuits are shown below.

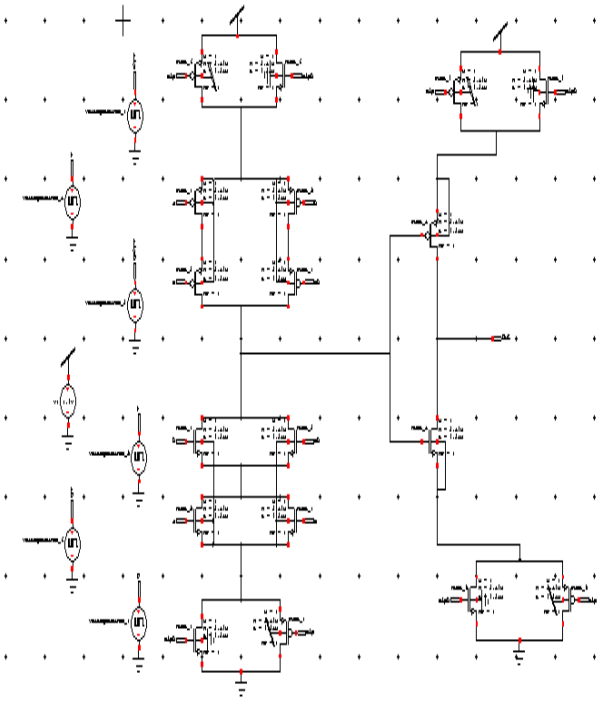

Fig. 6. 2x1 Multiplexer (LPSR Technique)

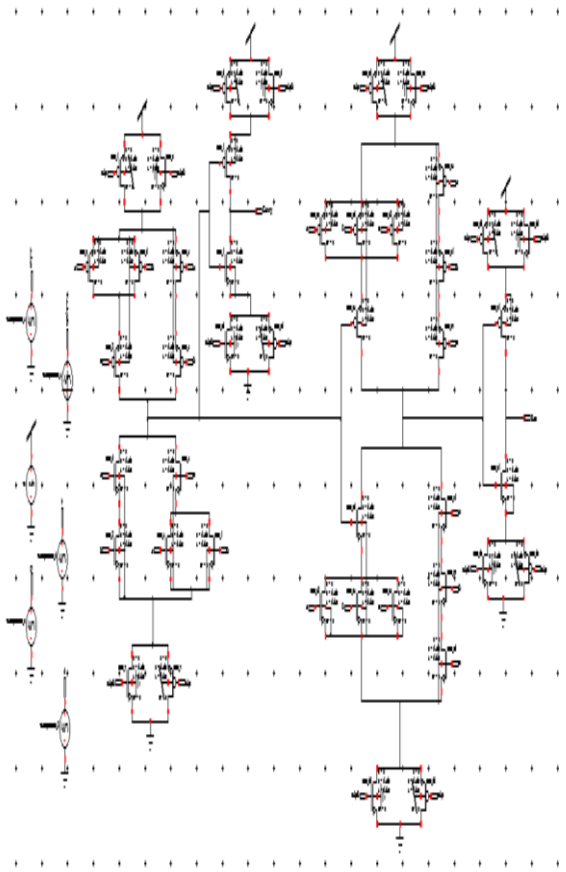

Fig.9. Full Adder (LPSR Technique)

V. SIMULATION AND RESULTS

All the data path elements are designed, simulated and functionally verified using 180nm technology files in Tanner EDA tool. Single VT transistors are used in all designs to show the performance benefits and comparison of different techniques. The logical functionality of each design is verified for all input combinations. Static power dissipation is calculated for all input combinations during active and sleep (idle) mode, also dynamic power during clocked operation are all measured using Tanner EDA tools. For pulsed operation transition period is taken as 30µs whereas the static power dissipation is measured for 20 µs duration. All the circuits are controlled by the sleep signals of same pulsed width and period is taken for the purpose of comparison.

Sleep control signals slp and slpb hold the respective leakage control transistors in the ON state during Active mode and during sleep mode the sleep control signals switch OFF the leakage control transistors.

The LPSR technique is proposed in this section to reduce the leakage power and total power dissipation to a maximum possible extent. The LPSR technique makes use of a pair of NMOS and PMOS transistors in the pull-up and pull-down paths of a CMOS circuit. Fig.5 shows the general block diagram of LPSR circuit.

Table I and Table II provides the dynamic power dissipation, static power dissipation for output logic-1 and logic-0, during active and sleep modes for all 2x1 Multiplexer and Full Adder respectively.

TABLE I Power Analysis for 2x1 Multiplexer

Technique	Dynamic Power Dissipation	Static Power Dissipation For Logic 1	Static Power Dissipation For Logic 0
LECTOR	3.1389µw	75.927pw	82.389pw
GALEOR	8.3809µw	1.0897µw	0.3331µw
Sleepy Keeper sleep mode	150.69pw	14.868pw	53.22pw
Sleepy Keeper active mode	2.4801µw	100.45pw	103.30pw
Sleepy Pass sleep mode	271.34pw	10.129pw	6.45pw
Sleepy Pass active mode	3.2457µw	93.969pw	83.856pw
LPSR sleep mode	16.255pw	4.2275pw	10.713pw
LPSR active mode	2.3129µw	100.45pw	103.30pw
LPSR state retention mode1	34.492nw	96.613pw	61.044pw
LPSR state retention mode0	40.199nw	59.875pw	105.62pw

TABLE IIIII POWER ANALYSIS FOR FULL ADDER

Technique	Dynamic Power Dissipation	Static Power Dissipation For Logic 1	Static Power Dissipation For Logic 0
LECTOR	8.9959µw	153.67pw	157.69pw
GALEOR	16.257µw	2.0792µw	0.6064µw
Sleepy Keeper sleep mode	2.3983nw	165.81pw	240.64pw
Sleepy Keeper active mode	5.6260µw	196.84pw	200.64pw
Sleepy Pass sleep mode	11.368nw	68.897pw	216.13pw
Sleepy Pass active mode	8.0353µw	170.92pw	174.72pw
LPSR sleep mode	5.0518nw	76.404pw	16.185pw
LPSR active mode	6.6639µw	196.84pw	200.64pw
LPSR state retention mode1	84.852nw	181.29pw	118.34pw
LPSR state retention mode0	129.14nw	122.22pw	188.85pw

VI. CONCLUSION

LECTOR and GALEOR techniques provide maximum leakage reduction during active mode of operation. But they suffer from maximum power dissipation during pulsed operation as they do not have sleep mode of operation. The Sleepy – Pass Gate technique has large power dissipation during pulsed operation. Though Sleepy Keeper technique maintains state during sleep mode at reduced levels, it results in large power dissipation during pulsed operation because the output terminal is permanently connected to leakage control circuit and there is no deep sleep state. The proposed LPSR technique has active mode static power on par with other techniques and it has least static power dissipation during deep sleep mode and retains state at low power. Thus the LPSR technique provides new choice for the designers of low power CMOS VLSI circuits.

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